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| EXAMINER | |
|---|---|
| RIZK, SAMIR WADIE | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/733,693 | BRITSON ET AL. | |
| | Examiner | Art Unit | |
| | SAM RIZK | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6,8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-20* is/are allowed.

6)☒ Claim(s) *1-4,6,8,9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

- Response to the Pre-Brief Appeal Conference to Re-Open Prosecution dated 12/20/2008
- Claims 5 and 7 have been Cancelled
- Claims 1-4, 6 and 8-20 have been submitted for examination
- Claims 1-4, 6, 8 and 9 have been rejected
- Claims 10-20 have been allowed

***Remarks***

1. In view of the pre-brief appeal conference decision mailed on 12/20/2007, the rejections of the final office action mailed on 8/9/2007 are withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Watari US patent no. 4,894,708 and in further view of Liberkowski US patent no. 5,691,209 and in further view of Bimbai et al. US patent no. 6141782 (Hereinafter Bombal).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-4, 6, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watari US patent no. 4,894,708 (Hereinafter Watari) and further in view of Liberkowski US patent no. 5,691,209 (Hereinafter Liberkowski).

3. In regard to claim 1, Watari teaches:

- A method for testing an integrated circuit (IC).comprising:
- employing one of a plurality of input lines to receive a test signal for a processor;

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- employing one of a plurality of output lines to send a test result from the processor; and

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- if the test result is unsuccessful, performing at least one of:

(Note: col. 3, lines (23-26) in Watari) ..

However, Watari does not teach:

- selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor using a first selection signal; and

- selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor using a second selection signal.

Liberkowski in an analogous art that teaches lattice interconnect device for manufacturing multi-chip modules teaches:

- selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor using a first selection signal; and

(Note: FIG. 5 and col. 10, lines (46-48) and (60-64) in Liberkowski)

- selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor using a second selection signal.

(Note: FIG. 5 and col. 10, lines (46-48) and (60-64) in Liberkowski)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Liberkowski that comprise automatic switching of input/output lines (pins) with the teaching of Watari. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need for automatically and selectively correcting backplanes and input/output IC pins.

4. In regard to claim 2, Watari teaches:

- The method of claim 1 wherein employing one of the plurality of input lines to receive the test signal for the processor includes:

- applying the test signal to each of the plurality of input lines;

(Note: FIG. 2, any of reference characters ((1), (1, Ia), (8), (8a) in Watari)

- selecting one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- receiving the test signal for the processor from the selected input line.

(Note: FIG. 2, reference character (8a) in Watari)

5. In regard to claim 3, Watari teaches:

- The method of claim 1 wherein employing one of the plurality of output lines to send the test result from the processor includes:

- applying the test result to each of the plurality of output lines;

(Note: FIG. 2, any of reference characters ((1), (1,1a), (8), (8a) in Watari) -

- selecting one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- sending the test result from the processor using the selected output line.

(Note: FIG. 2, reference character (8a) in Watari)

6. In regard to claim 4, Watari teaches:

- The method of claim 1 wherein employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

- selecting a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of input lines to Receive the test signal.

(Note: FIG. 2, reference character (8a) in Watari)

7. In regard to claim 6, Watari teaches:

- The method of claim 1 wherein employing a remaining one of the plurality of output lines to send the test result from the processor includes:

- selecting a remaining one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 2, reference character (8a) in Watari)

8. In regard to claim 8, Watari teaches:

- The method of claim 1 wherein:

- employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

- selecting a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of input lines to receive the test signal; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing a remaining one of the plurality of output lines to send the test result from the processor includes:

- selecting a remaining one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 2, reference character (8a) in Watari)

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watari/Liberkowski as applied to claim 8 above, and further in view of Bombai et al. US patent no. 6141782 (Hereinafter Bombai).

10. In regard to claim 9, Watari/Liberkowski teaches substantially all the limitations in claim 8. and the limitations of claim 9 that:

- selecting a remaining one of the plurality of input lines includes: selecting a remaining one of the plurality of input lines based on the modified first select signal; and

(Note: FIG. 5 and col. 10, lines (46-48) and (60-64) in Liberkowski)

- selecting a remaining one of the plurality of output lines based on the modified second select signal.

(Note: FIG. 5 and col. 10, lines (46-48) and (60-64) in Liberkowski)

However, Watari/Liberkowski does not teach:

- modifying a first select signal; and
- modifying a second select signal; and

Bombai in an analogous art that teaches pseudo-scan using hardware accessible IC structures teaches:

- selecting a remaining one of the plurality of input lines includes:
- modifying a first select signal; and

(Note: FIG. 8, third and forth step in.Bombai) and

- modifying a second select signal; and

(Note: FIG. 8, third and forth in Bombai)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Watari that teaches parallel I/0 testing of an IC with the teaching of Bombai.

This modification would have been obvious to one of ordinary, skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need for an efficient IC fault coverage.

***Allowable Subject Matter***

11. Claims 10-20 have been allowed.

**REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance:

12. The prior Art of record and in particular Watari/Liberkowski/Bombal teach IC and lattice interconnect for multi-chip modules. However, the prior art do not teach, suggest, or otherwise render obvious the limitations recited in claim 10 that:

- An apparatus for testing an IC comprising:
- a **processor** within the IC;
- a plurality of input lines coupled to the processor **positioned internally within the IC**;
- a plurality of output lines coupled to the processor **positioned internal within the IC**; and
- a connector interface coupled to the plurality of input lines and the plurality of output lines;
- wherein the apparatus is adapted to:
- employ one of the plurality of input lines to receive a test signal for the processor;
- employ one of the plurality of output lines to send a test result from the processor; and
- if the test result is unsuccessful, perform at least one of:

13. Claims 11-20 depend from claim 10.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Madurawe US patent no. 7239174 and US publication no. 2005/0162933 teaches programmable interconnect structures for routing signals in PLD IC devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

/Sam Rizk/

Examiner, Art Unit 2112

/JACQUES H LOUIS-JACQUES/

Supervisory Patent Examiner, Art Unit 2112